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Power Dissipation of NAND Gate based CMOSMultiplexer using Sleepy Keeper Technique

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Abstract: - As a consequence of the Moore's law, every year channel length of the MOSFET is reducing, causing Short Channel Effect (SCE). SCE is effecting the performance of the circuit designed using the low dimensional MOSFETs. High frequency performance and power consumption of the circuits is largely affected due to SCE. In today's world of consumer electronics there is a requirement of high frequency circuits which is having low power consumption so that it can be used in designing battery driven handheld devices. On the other hand there is a huge requirement of CMOS technology compatible device which can be used as poweramplifiers for communication devices like repeaters and routers. NAND gates is implemented using various technique approaches for digital schematic design such as sleepy keeper, stack approach, sleepy keeper etc. Power utilization analysis of the various method techniques for NAND gates is implemented. To implement and power utilization is analysis for NAND gates using sleepy keeper approach and comparing with various existing methods. It is also implement CMOS multiplexer using NAND gate and optimize power dissipation. The CMOS circuits is implementing DSCH and draw the layout of MICROWIND software.

Keywords: CMOS, NAND Gate, Sleepy Keeper, DSCH, MICROWIND

I. INTRODUCTION

Reducing power dissipation has now become a critical design concern in almost all electronic systems. Reduction in the supply voltage is the most significant method for reducing the power dissipation because of thequadratic relationship between the supply voltage and the dynamic power dissipation [1]. To compensate for theperformance loss due to a lower supply voltage, threshold voltage of MOS transistors is also reduced. However, this causes an increase in the leakage current. Among all leakage currents, sub threshold leakage current is the most dominant [2]. This leakage current will become a large component in the total power dissipation with further down scaling in technology. Therefore, today an important research area in achieving low power dissipation is to develop effective circuit techniques to reduce this leakage current that is mainly caused by the reduction in the threshold voltage of MOS transistors and down scaling in technology (Roy et al. 2003). Technology scaling has allowed more functions per unit area, and lower dynamic power dissipation, but has alsoincreased the leakage power dissipation exponentially. An analysis of trends based on the International Technology Roadmap for Semiconductors (ITRS) shows that the leakage power dissipation is beginning to exceed the dynamic power dissipation with the down scaling in technology generation, which is shown in Fig.

1.1. In the past, circuit design techniques and architectures ignored the effects of leakage power dissipation because it was insignificant in comparison with the dynamic power dissipation. However, in modern technologies, the role of sub threshold leakage power dissipation cannot be ignored and now it has become dominant in the overall power dissipation in deep submicron and Nano-scale technologies [3, 4].

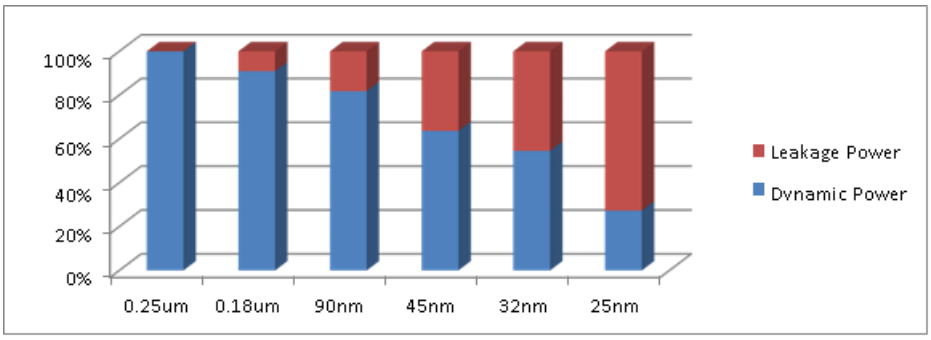


Figure 1: Leakage versus dynamic power dissipation trends with technology scaling

Although total power dissipation (dynamic and leakage) during the active mode is reduced with the scaling in the supply voltage, further power dissipation can only be reduced if standby leakage power dissipation is controlled wherever possible, since this leakage power will make up a larger percentage in the overall power dissipation with further scaling down in technology [5].

II. POWER DISSIPATION IN CMOS

The power dissipation of CMOS circuits are usually comprised of three components namely Static power dissipation (SPD), Dynamic power dissipation (DPD) and Short circuit power dissipation (ScPD). The total power dissipation is represented by

$$Total\ power\ dissipation = SPD + DPD + ScPD \quad (1)$$

Reverse biasing, the diffusion area, and the CMOS transistor's surface are all major contributors to the static power loss. In most cases, leakage current and voltage supply are used to define SPD. However, the capacitance's charging and discharging creates the dynamic power dissipation. Dropping the load capacitor or rail voltage (Vdd) can make it intense. The navigation path that runs in the middle of the rail voltage (Vdd) and ground results in power loss during a short circuit. Power indulgence is primarily disrupted by sub-threshold leakage, gate-oxide excavation, and reverse bias intersection as a result of technological advancement. By disrupting the minimum voltage, increasing gate oxide thickness increases sub-threshold current and intensifies gate oxide tunneling current [6, 7].
The primary sources of power loss are:

1) The loss of capacitive power as a result of the load capacitance's charging and discharging;
2) Short circuit currents because there is a conducting path between the voltage supply and ground during a logic gate's brief transition; and
3) Current leakage. Sub-threshold and reverse-bias diode currents make up the leakage current.

The first is the result of stored charge between the active transistor drain and bulk, and the second is the result ofcarrier diffusion between the OFF transistor source and drain. By designing the circuit to have equal input and output rise/fall edge times, the short-circuit power dissipation can be reduced to 10% of the total power dissipation. Technology processes with feature sizes greater than 1 m are dominated by power dissipation from switching activity. As technology processes progress toward the deep-submicron regime, transistor feature sizes are shrinking, lowering load capacitances. The supply voltage must also be reduced as a result of the smaller feature size. For dynamic power savings, the voltage scaling method makes use of the quadratic dependence of switching power on supply voltage. However, this method incurs a cost for the operation of the circuit by significantly increasing the delay as the supply voltage approaches the devices' threshold voltage [8, 9].

III. PROPOSED METHODOLOGY

This section explains the structure of the sleepy keeper approaches well as how it operates. In addition, we discuss some layout issues for the sleepy keeper approach. The basic problem with traditional CMOS is that the transistors are employed in their effective manner. PMOS transistor is applied with VDD supply and NMOS transistor is grounded.

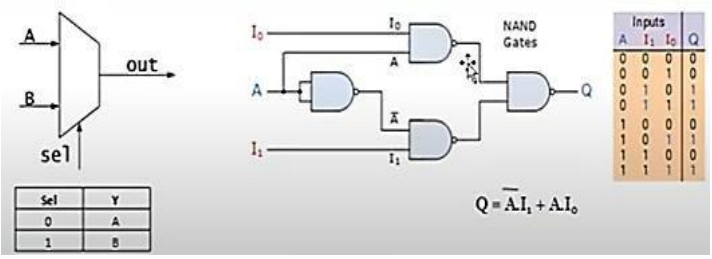


Figure 2: 2:1 MUX using NAND Gate

However the PMOS transistors are not effective while dispatching GND. Similarly the NMOS transistors arenot effective at passing VDD. In order to uphold the level „1" during sleep state, the sleepy keeper technique utilizes the output value of „1". An NMOS transistor is connected to VDD so that the output value is maintained to „1" during sleep state. A supplementary single NMOS transistor connected across the pull-up sleep transistor passes VDD to pull up network.

During sleep state, this NMOS transistor is the only source of VDD as the sleep transistor is kept off. As shown in Figure 3, an additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects VDDto the pull-up network. When in sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. As shown in figure 3.8, a supplementary single PMOS transistor is placed across the pull-down network. During sleep state, this NMOS transistor is the only source of VDD as the sleep transistor is kept off. It is the dual case of the output „1"case explained above. For this approach to work, all that is needed is for the NMOS connected to VDD and the PMOS connected to GND to be able to maintain proper logic state. This seems likely to be possible as other researchers have described ways to use far lower VDD values to maintain logic state. For example propose some significantly reduced VDD values sufficient to maintain state. We emphatically do not use sleepy keeper transistors (the NMOS connected to VDD and the PMOS connected to GND) to dynamically change the output voltage but instead only use them to maintain an already calculated output voltage. Specifically, only a few clock cycles after entering sleep to a few clock cyclesprior to leaving sleep do the sleepy keeper transistors acts as the sole connection to keep the output voltage unchanged.

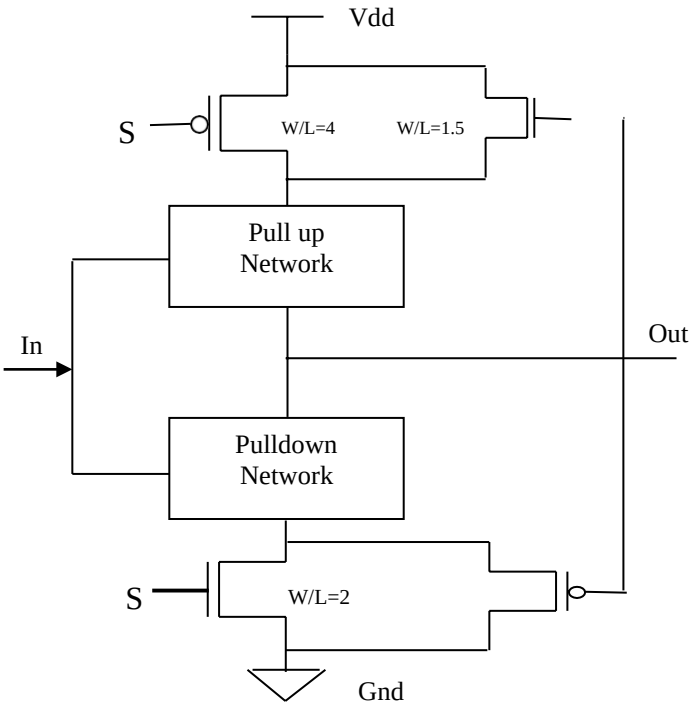


Figure 3: Sleepy keeper approach

IV. SIMULATION RESULTS

The proposed methodology is a sleepy keeper approach to reduce for power consumption. Here, the powerconsumption is observed by employing the DSCH and MICROWIND tool.

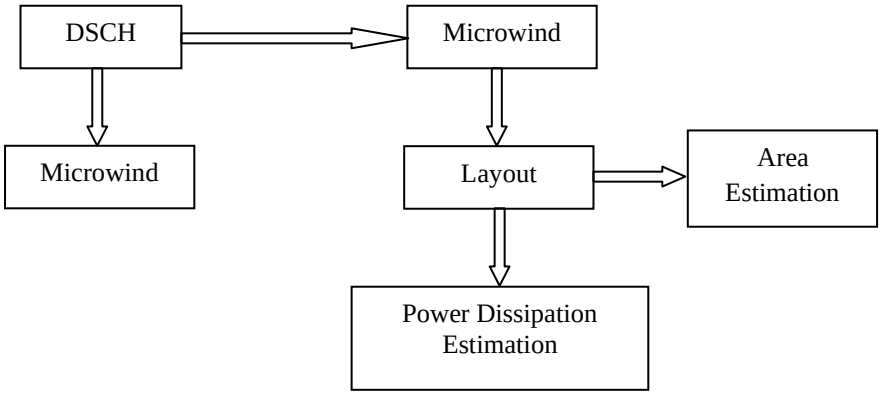
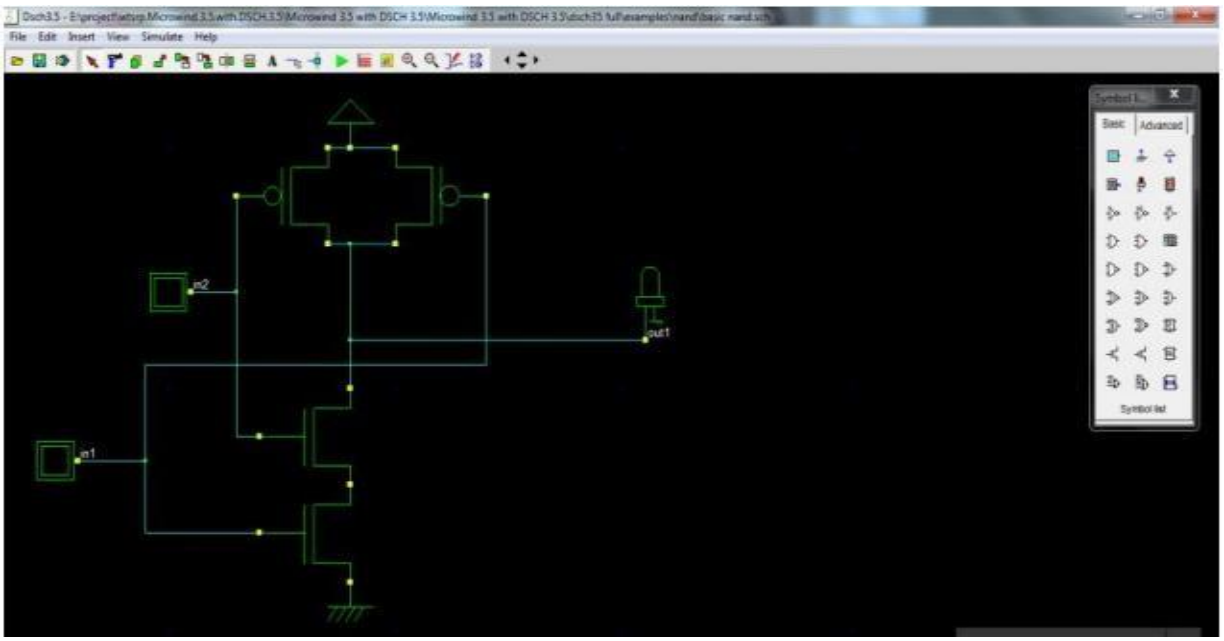


Figure 4: Block diagram



Designing Circuits the Figure 5 inferences the digital schematic diagram for basic NAND gate using microwindtool.

Figure 5: Design of basic NAND gate

The Figure 6 inferences the digital schematic diagram for Zigzag approach NAND gate using microwind tool.

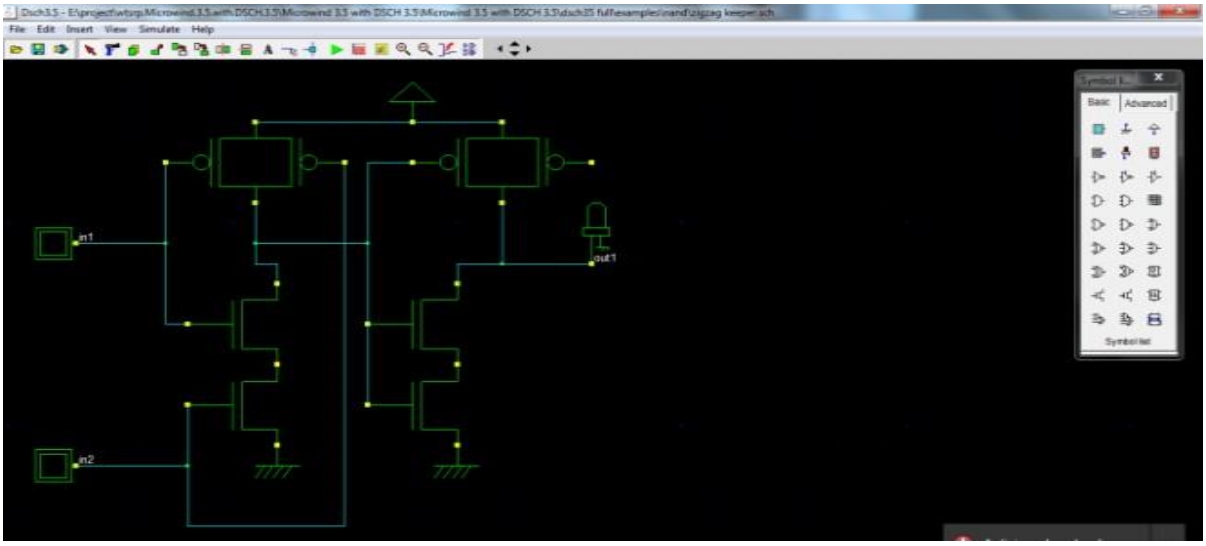


Figure 6: NAND gate using zigzag approach

The Figure 7 inferences the digital schematic diagram for dual stack approach NAND gate using microwindtool.

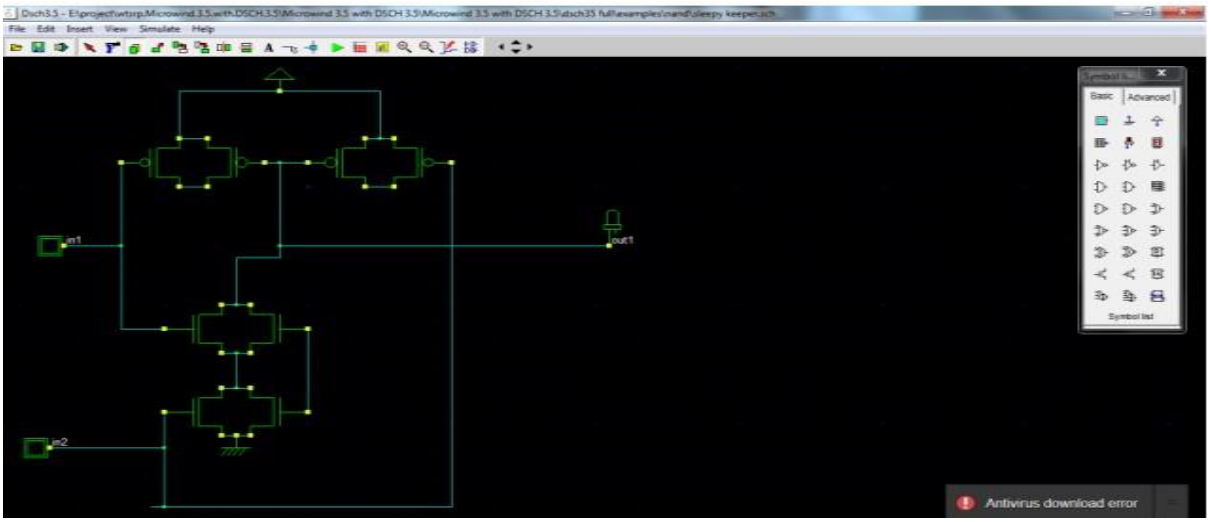


Figure 7: NAND gate using dual stack approach

The Figure 8 inferences the digital schematic diagram for sleepy keeper approach NAND gate using microwind tool.

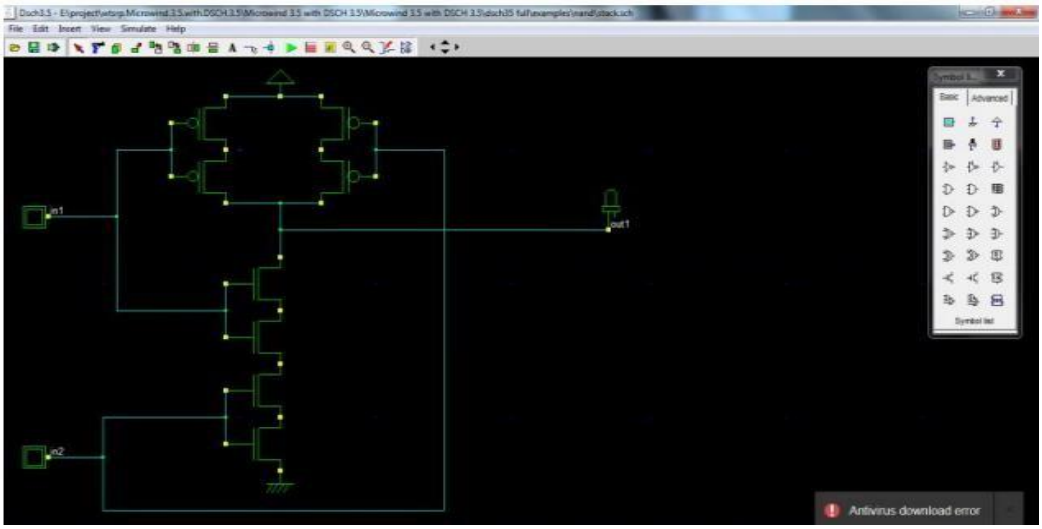


Figure 8: NAND using sleepy keeper approach

The power utilized by basic NAND gate is 14.016(µW). The power utilized by NAND using zigzag approach and dual stack is 2.328(µW) and 1.033(µW) respectively. The power utilized by NAND using stack and sleepy stack is 1.183 (µW) and 0.656 (µW) respectively. The power utilized by NAND using proposed sleepy keeper is0.595(µW). The power utilized by basic NOR gate is 1.437(µW).The power utilized by NOR using zigzag approach and dual stack is 1.347(µW) and 1.850(µW) respectively. The power utilized by NOR using stack and sleepy stack is 1.397(µW) and 0.706(µW) respectively. The power utilized by NOR using sleepy keeper is 0.644(µW). The Figure 9 inferences the power utilized by dual stack approach NAND gate using microwind tool.

Figure 9: Power utilized by dual stack approach NAND gate

The Figure 10 inferences the power utilized by sleepy keeper approach NAND gate using microwind tool.

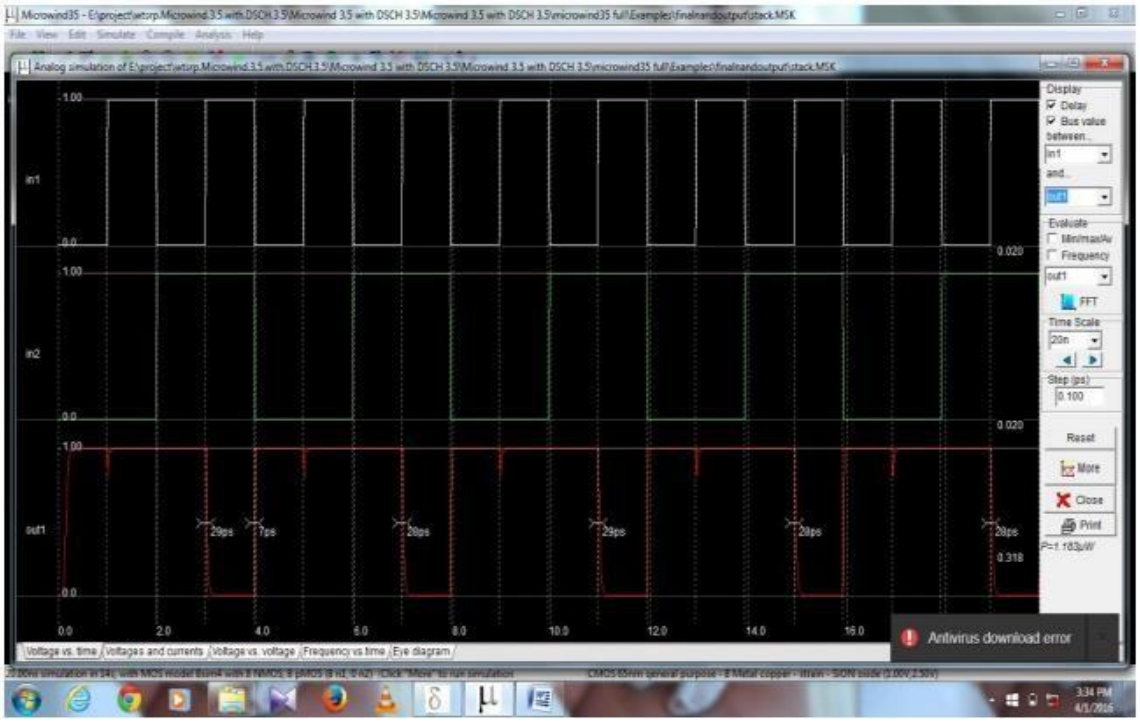


Figure 10: Power utilized by sleepy keeper NAND gate

Table 1 represents the NAND gate using different methods. The basic NAND gate provide a power of 3016 nW,Zigzag method provide a power 2328 nW, Stack method provide a power 1183 nW, Dual Stack method providea power 1033 nW, Sleepy Stack method provide a power 696 nW and Sleepy Keeper method provide a power 595 nW. Fig. 5.22 shows the graphical representation of the comparison method.

Table 1: Comparison of power utilization of NAND gate using various methods

Method	Power (nW)	
	Previous Sai Srinivas Chandra et al. [1]	Proposed Method
Basic Nand Gate	4036 nW	3016 nW
Zigzag Method	2893 nW	2328 nW
Stack Method	1467 nW	1183 nW
Dual Stack Method	1282 nW	1033 nW
Sleepy Stack Method	899.3 nW	696 nW
Sleepy Keeper Method	829.7 nW	595 nW

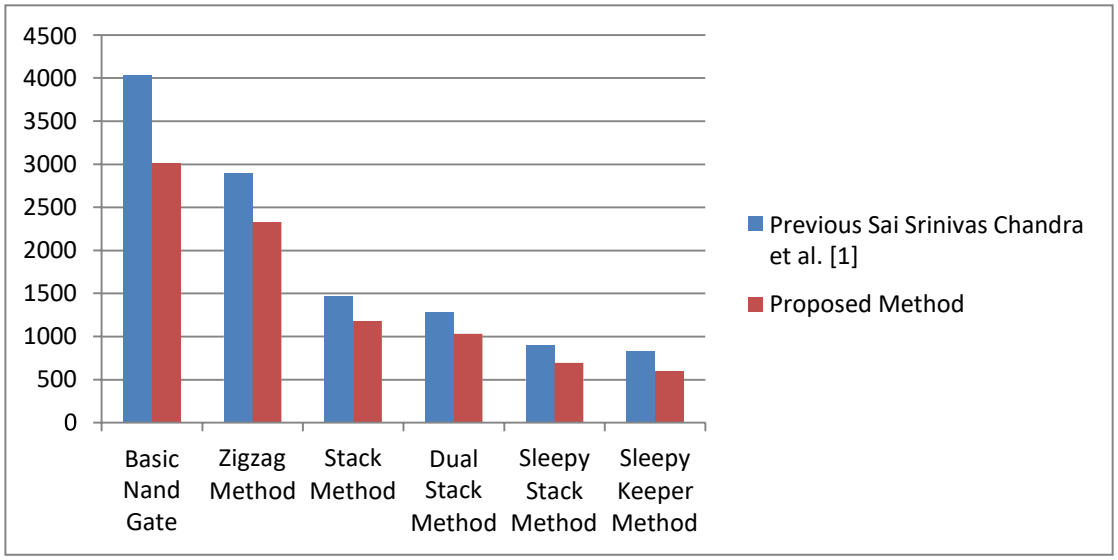


Figure 11: Graphical Represent of NAND Gate

V. CONCLUSION

This method includes producing a numerous primary inputs, appraising the leakage of each input, and possession track of the best vector providing the minimal leakage current. A more well-organized way is to employ the genetic algorithm to exploit historical data to speculate on new search points with expected improved performance to find a near-optimal solution. The reduction of standby leakage power by application of an input vector is a very operational method of monitoring the sub threshold outflow in the standby mode of operation of a circuit. In a stack transistor insertion technique is given. For the gates with high sub threshold leakage in non-critical paths, a Leakage Control Transistor (low) is inserted in series and is turned off during thestandby mode. The technique can effectively diminish the leakage current by means of single-threshold voltage. We here review previously proposed circuit level approaches for sub threshold leakage power reduction. The most well-known traditional approach is the sleep approach.

LIST OF ABBREVIATION

S.No	Abbreviation	Definition
1	MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
2	SCE	Short Channel Effect
3	CMOS	Complementary Metal Oxide Semiconductor
4	NAND	NOT AND
5	DSCH	Digital Schematic Circuit Designing software
6	MOS	Metal Oxide Semiconductor
7	ITRS	International Technology Roadmap for Semiconductors
8	SPD	Static power dissipation
9	DPD	Dynamic power dissipation
10	ScPD	Short circuit Power Dissipation
11	PMOS	p-channel Metal Oxide Semiconductor
12	NMOS	n-channel Metal Oxide Semiconductor

DECLARATIONS

1. **Funding Declaration**

I, Priya Verma, first author of the research paper, hereby declare that I did not receive support from any organization for the submitted work. No funding was received to assist with the preparation of this.

2. **Data Availability Declaration**

I, hereby declare that this research paper is a part of dissertation of my Ph.D. So complete data can be accessed after completion of it.

3. **Competing Interest Declaration**

I, hereby declare that I have no competing interest that could appear to influence the work reported in this paper.

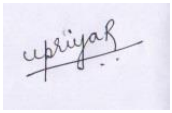
4. **Consent to publish Declaration**

"Not Applicable"

5. Author's Contribution

Study conception and design: Priya Verma; Data collection: Dr. Mukesh Tiwari; Analysis and interpretation of results: Dr.Mukesh Tiwari, Er. Priya Verma; Draft manuscript preparation: Er. Priya Verma. Both authors reviewed the results and approved the final version of the manuscript.

First Author: Priya Verma



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