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Optimize Power of CMOS Multiplexer based NOR Gate using Sleepy Stack Technique

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Abstract: - In Deep Submicron CMOS digital circuits, analytical analysis of circuit performances, such as thepower dissipation and delay, is an important issue. The speed and power consumption trade off against eachother. In general, if the speed has top priority, the threshold voltage is reduced and the supply voltage isincreased; if the power dissipation has top priority, the threshold voltage is increased and the supply voltage isdecreased. In this paper, the analysis of CMOS multiplexerbased NOR gate using different technique. ToSurvey the various existing research works that are relevant to the proposed research work such as sleepy stack,dual stack, zigzag, forced stack etc.To analyze the power gating and multi-threshold CMOS circuits, inputvector control and data driven clock circuits that are relevant to the proposed sleepy stack technique. The CMOScircuitisimplementing DSCHanddrawthelayoutofMICROWIND software.

Keywords:CMOS,NORGate,SleepyStack,DSCH,MICROWIND

I. INTRODUCTION

The technological innovations show a very high growth rate, which develop highly sophisticated computingdevices with the feature of processing them by the user from the place wherever they want. In addition, the usersrequire very high speed operation andalso expect the devices must be low-priced. These requirements havesome constraints regarding the size and power consumption of the devices. The portable and high-speed deviceslike cell phones, laptop requires lower power consumption circuits [1, 2]. The modern cell phones transmit thevoicealongwiththedata.Theyrequirecomplicatedvideoprocessingmethodsandspeechrecognitionalgorithms.
Hence, these processes like video compression and decompression, speech compression, accessingthe multimedia files consume more power than the devices not having these features [3]. The size reduction ofthe circuit leads to the high-density package and hence the overriding problem occurs with the transistors. It isnot a feasible solution to merely reduce the size for attaining low power consumption in electronic circuits.Therefore a highly efficient architecture is required to fabricate the modern electronic devices low powerconsumption. Very Large Scale Integration (VLSI) is a technology used to fabricate the devices with less sizeand less weight. Much architecture has been developed in VLSI technology to obtain less weight and high speeddeviceswithlowpowerconsumption[4, 5].
Since the modern electronic devices like computers, laptops, mobile phones need to perform highly complexoperations; their processing speed and the battery lifetime must be high. When performing the multi-operationsat a time, the battery power drains and also the device gets heated. So the devices must be fabricated with thecircuits requiring less power. Since the power dissipation of the circuit varies in proportion with the supplyvoltage, the supply voltage must be made low in order to reduce the power dissipation problem. In contrary,while decreasing the supply voltage, the speed of the logic circuit decreases. Hence, to overcome this adverseprocess, the threshold voltage is made low [6]. But this process results in more leakage or standby powerdissipation because of the sub threshold current flow through the MOSFETs. Even the presence of very lowthresholdswitchescancausethestandbyleakagepower.Asaresult,oneneedstocomputethepowerdissipation in a circuit by considering not only the dynamic power, also the standby power dissipation. Manymethods have been proposed to lower the leakage power in low threshold devices by making changes at thecircuitlevel andprocesslevel[7, 8].

II. LEAKAGEPOWER

Total leakage current of n-MOSFET in off-state is given as the summation of various leakage currents such asSub-thresholdleakagecurrent(ISTH),band-to-bandtunnelingleakagecurrent(IBBT),gate-induceddrainleakage current (IGID), gate-to bulk oxide tunneling leakage current (IGB), drain-to-oxide tunneling leakagecurrent (IDG).IBBT and IGID has two components. They are drain-to-bulk and source-to-bulk reverse-bias p-njunctionleakage currents.

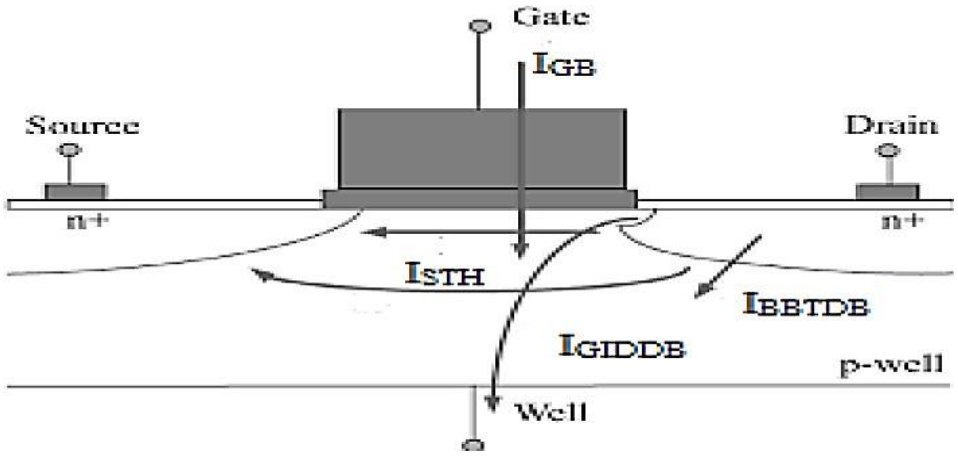


Figure1:Standbyleakagecurrent ofMOSFET

The MOSFET is said to be in off-state when it is working below the threshold voltage, (gate-to-source voltage,(VGS=0). Still a small amount of current passes through the device in off-state which causes significant powerdissipation in the device. So it is very essential to select the value for sub-threshold leakage current (ISTH).ISTH is the weak reverse conduction current and controlled by the diffusion current passing across drain andsource when VGS is less than V_{th} [11]. The electric field intensity across the depletion region becomes high dueto the raise of IBBT caused by heavy doping of Source/drain and substrate region. If this electric field becomesgreater than 106 V/cm, the voltage drop across the junction is greater than the silicon band- gap and hence theenormousamountofIBBTpassesacrosssubstratejunctions[12].Assaidintheabovesection,IGIDisduetothe IBBT in the high field depletion region in the gate-drain overlap region. The depletion region is formed bybiasing drain at supply voltage (Vdd) and gate at 0V. Similar to IBBT large amount of IGID passes across drain-to-substrate junctions because of band rotation, when the high electric field is created in the narrow depletionregiondue toreverse biasbetweenchannelanddrain.

III. PROPOSEDMETHODOLOGY

However, separated transistors shows more delay and restrict the usefulness of the technique. The sleepy stackmethod conjoins the sleep and stack techniques. Similar to the stack technique, the sleepy stack splits the normaltransistors into two half sized transistors. Afterwards sleep transistors are inserted in parallel with any of theseparated transistors. In sleep state, sleep transistors are switched off and stacked transistors suppress leakagecurrent in saving mode. Each sleep transistor cuts down the resistance of the path, and therefore the delay isreduced during active state. However the efficiency attained with this approach is only 30%. However, areapenalty is a significant matter for this approach since every transistor is replaced by three transistors and sinceadditionalwiresare added forSandS',whichare sleepsignals.

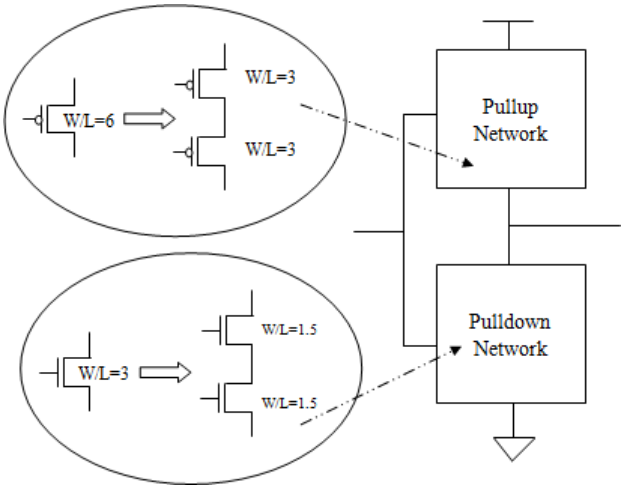


Figure2:SleepyStackapproach

In sleep mode, both the sleep transistors are kept off and one of the transistors in across with the sleep transistorsis connected with the suitable power rail. In the sleep approach, zigzag approach, sleepy stack approach andleakage feedback approach, dual V_{th}method can be employed to get greater leakage power reduction. Highvalue of threshold voltage causes less leakage and less performance, hence high threshold voltage is given to theleakage reduction transistors only, which are sleep transistors, and low threshold voltage is given to the othertransistors to preserve logic performance. The delay is reduced in this technique and the drawback is therequirementoflargespace.

IV. SIMULATIONRESULTS

The proposed methodology is a sleepy keeper approach to reduce for power consumption. Here, the powerconsumptionisobservedbyemployingthe DSCH andMICROWIND tool.

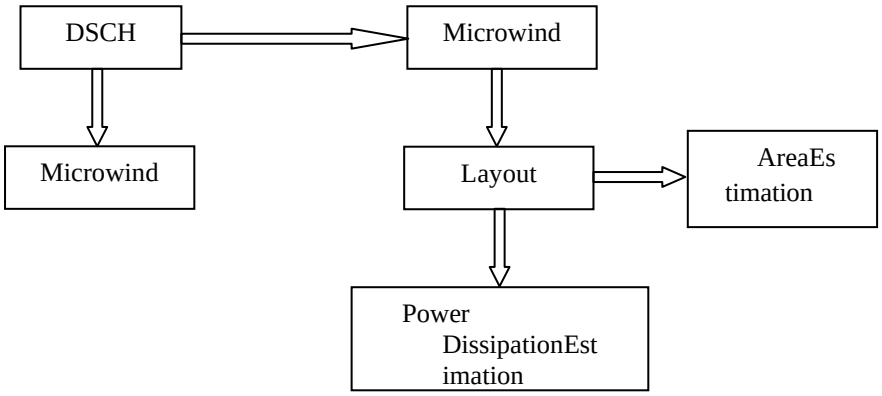


Figure3:Blockdiagram

TheFigure4 inferencesthedigitalschematicdiagramforbasicNORgateusingmicrowindtool.

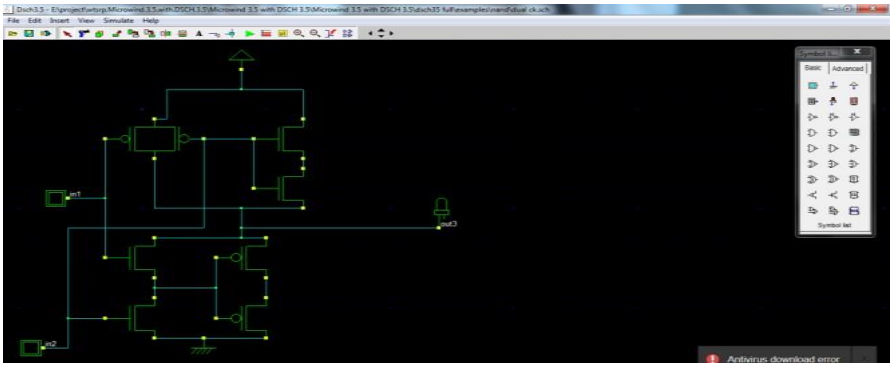


Figure4: BasicNORgate

TheFigure5 inferencesthedigitalschematicdiagramforstackapproachNORgateusingmicrowindtool.

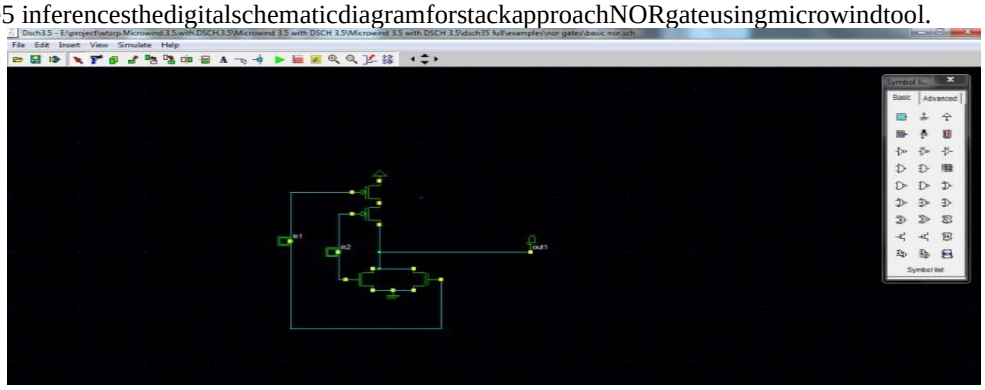


Figure5: NORgateusingstackapproach

TheFigure6 inferencesthepower utilizedbybasicNORgateusingmicrowindtool.

Figure6:PowerutilizedbybasicNORgate

Figure7:Powerutilizedbydual stackapproachNAND gate

TheFigure8 inferencesthepowerutilizedbyzigzagapproachNOR gateusingmicrowindtool.

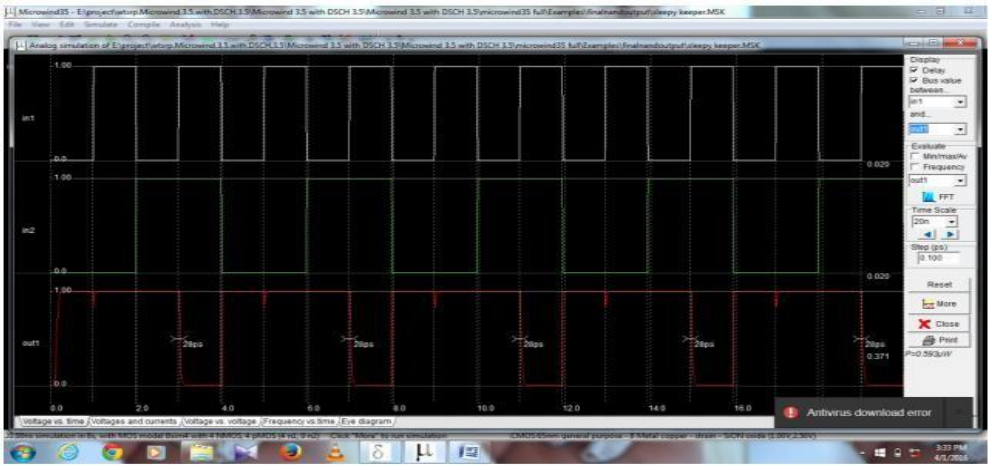


Figure8:Power utilizedbyzigzagapproach NORgate

TheFigure9 inferencesthepowerutilized bysleepystackapproachNORgateusing microwind tool.

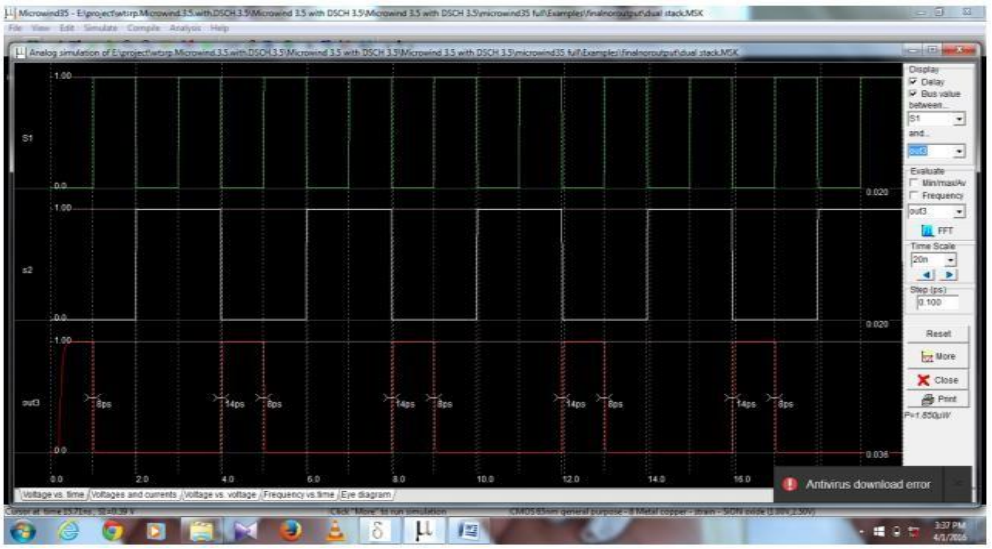


Figure9:Power utilizedbysleepystackNORgate

Table 1 represents the NOR gate using different methods. The basic NOR gate provide a power of 1437 nW,Zigzag method provide a power 1374 nW, Stack method provide a power 1397 nW, Dual Stack method provideapower1250nWandSleepyStackmethodprovideapower706nWFig.10showsthegraphicalrepresentationoft hecomparisonmethod.

Table1:ComparisonofpowerutilizationofNORgateusing variousmethods

Method	**Power(uW)**	
	PreviousSaiSrinivas Chandraetal.[1]	ProposedMethod
BasicNORGate	1892 nW	1437nW
ZigzagMethod	1782 nW	1374nW
StackMethod	1626 nW	1397nW
DualStackMethod	1472 nW	1250nW
SleepyStackMethod	902.3nW	706nW

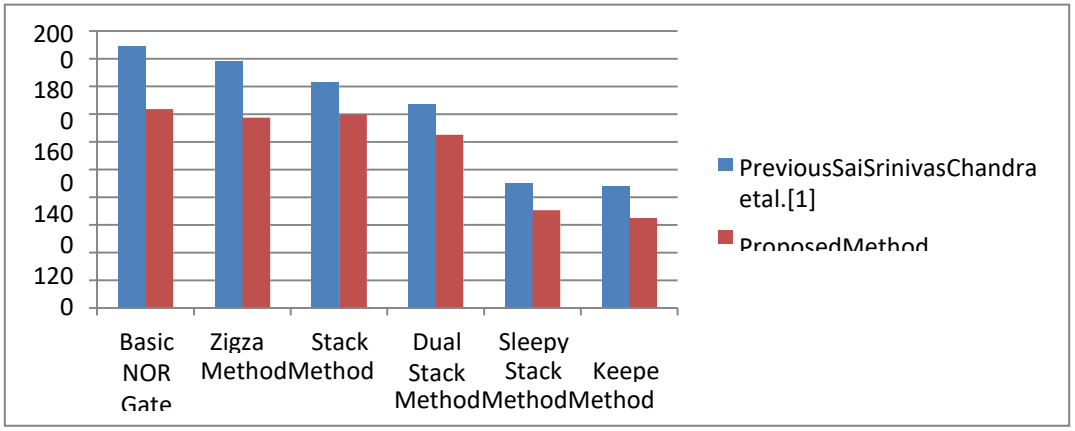


Figure10:GraphicalRepresentof NORGate

V. CONCLUSION

Due to the stacking effect, the sub threshold leakage over a logic gate be subject to on the applied input vector.This tends to create the total leakage current of a circuit in need of on the states of the primary inputs. The moststraightforward way to determine a low leakage input vector is to compute every combination of primary inputs.For a circuit with primary inputs, there are combinations for input states. Owing to the exponential difficultywithrespecttothenumberofprimaryinputs,likeexhaustivemethodislimitedtocircuitswithasmallnumberof primary inputs. Meant for large circuits, a random search-based procedure can be used to observe the bestinput arrangements. This method includes producing a numerous primary inputs, appraising the leakage of eachinput,andpossessiontrackof the bestvectorprovidingtheminimal leakage current.

VI. LIST OF ABBREVIATION

S.No	Abbreviation	Definition
1	MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
2	SCE	Short Channel Effect
3	CMOS	Complementary Metal Oxide Semiconductor
4	NAND	NOT AND
5	DSCH	Digital Schematic Circuit Designing software
6	MOS	Metal Oxide Semiconductor
7	ITRS	International Technology Roadmap for Semiconductors
	SPD	Static power dissipation
9	DPD	Dynamic power dissipation
10	ScPD	Short circuit Power Dissipation
11	PMOS	p-channel Metal Oxide Semiconductor
12	NMOS	n-channel Metal Oxide Semiconductor

DECLARATIONS

1. **Funding Declaration**
I, Priya Verma, first author of the research paper, hereby declare that I did not receive support from any organization for the submitted work. No funding was received to assist with the preparation of this.

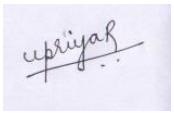
2. **Data Availability Declaration**
I, hereby declare that this research paper is a part of dissertation of my Ph.D. So complete data can be accessed after completion of it.

3. **Competing Interest Declaration**
I, hereby declare that I have no competing interest that could appear to influence the work reported in this paper.

4. **Consent to publish Declaration**
"Not Applicable"

5. Author's Contribution
Study conception and design: Priya Verma; Data collection: Dr. Mukesh Tiwari; Analysis and interpretation of results: Dr.Mukesh Tiwari, Er. Priya Verma; Draft manuscript preparation: Er. Priya Verma. Both authors reviewed the results and approved the final version of the manuscript.

First Author: Priya Verma



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